OIPE
MAR 2 2 2004
PATENT & TRADEMARK OFFICE

TRANSMITTAL LETTER (General - Patent Pending)	Docket No. 51889/3

In Re Application Of: **Douglas R. Hackler, Sr. et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
10/719,119	November 21, 2003	Not yet assigned	2814

Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Information Disclosure Statement
PTO-1449 with copies of cited articles
Postcard

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☐ The Director is hereby authorized to charge and credit Deposit Account No. as described below.
  - ☐ Charge the amount of
  - ☐ Credit any overpayment.
  - ☐ Charge any additional fee required.

John R Thompson
Signature

Dated: **March 18, 2004**

John R. Thompson
Registration No. 40,842
STOEL RIVES LLP
One Utah Center
201 South Main Street, Suite 1100
Salt Lake City, UT 84111
Phone: (801) 578-6994; Facsimile: (801) 578-6999

cc:

I certify that this document and fee is being deposited on **March 18, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

John R Thompson
Signature of Person Mailing Correspondence

John R. Thompson
Typed or Printed Name of Person Mailing Correspondence

OIPE JC116
MAR 2 2 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Douglas R. Hackler, Sr. et al. Confirmation No. 1799

Application No. 10/719,119

Filed: November 21, 2003

For: **DOUBLE-GATED TRANSISTOR CIRCUIT**

Group Art Unit: 2814

Examiner:

Date: March 18, 2004

INFORMATION DISCLOSURE STATEMENT

TO THE COMMISSIONER FOR PATENTS:

1. Pursuant to the duty of disclosure, documents listed on the accompanying Form PTO-1449 (or equivalent) are presented for the Examiner's consideration.

   ☒ Copies of listed documents are enclosed. (37 CFR § 1.98(a))

   ☒ Copies of listed U.S. patent documents are omitted because this application was filed after June 30, 2003 and is, thus, subject to image file wrapper processing. Copies of listed foreign patent documents and non-patent literature are enclosed.

   ☐ Copies of the documents listed on sheet(s) _____ of Form PTO-1449 (or equivalent) are omitted because (1) they are already of record in U.S. Patent Application No. _____, filed _____, on which this application relies for an earlier filing date under 35 U.S.C. § 120; and (2) any information disclosure statement filed in the prosecution of Application No. _____, complies with 37 CFR §§ 1.98(a) through (c). (37 C.F.R. § 1.98(d))

2. ☐ The Examiner's attention is directed to the enclosed copy of copending U.S. Patent Application No. _____, filed _____, for _____, which is cited in this application.

3. This information disclosure statement is being submitted (check box a., b., or c.):

   a. ☒ Within three months of the filing date of a national application or entry of the national stage in an international application; or before the mailing of a first Office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. (No statement under 37 CFR 1.97(e) is required.); or

OIPE JC116
MAR 2 2 2004
PATENT & TRADEMARK OFFICE

b. ☐ After the period set forth in paragraph 3a, but before the mailing date of either a final action, a notice of allowance, or an action that otherwise closes prosecution in the application. (Check box i. or ii.)

i. ☐ A $180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed, or

ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below; or

c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of the issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. Enclosed is a $180.00 information disclosure statement processing fee set forth in 37 CFR 1.17(p).

4. If a statement specified by 37 CFR 1.97(e) is required, the attorney or agent signing below hereby states that:

☐ each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.

5. ☐ A concise explanation of the relevance of each document not in the English language and/or selected documents in the English language is set forth below.

Respectfully submitted,

By _____
John R. Thompson
Registration No. 40,842

STOEL RIVES LLP
One Utah Center Suite 1100
201 S Main Street
Salt Lake City, UT 84111-4904
Telephone: (801) 328-3131
Facsimile: (801) 578-6999
Attorney Docket No. 51889/3

OIPE
MAR 2 2 2004
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (REV. 7-80)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.	APPLICATION NO.
51889/3 US	10/719,119

INFORMATION DISCLOSURE CITATION

APPLICANT – Douglas R. Hackler, Sr. et al.

Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**

FILING DATE-
November 21, 2003

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
	2	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	07/02/02
	3	2002/0140039 A1	10/03/02	Adkisson et al.	257	377	06/18/02
	4	2002/0105039 A1	08/08/02	Hanafi et al.	257	401	02/07/01
	5	2002/0093053 A1	07/18/02	Chan et al.	257	347	01/18/02
	6	2003/0089930 A1	05/15/03	Zhao	257	256	11/07/02
	7	6,580,137 B2	06/17/03	Parke	257	401	08/29/01
	8	6,518,127 B2	02/11/03	Hshieh et al.	438	270	06/01/01
	9	6,506,638 B1	01/14/03	Yu	438	156	10/12/00
	10	6,483,156 B1	11/19/02	Adkisson et al.	257	401	03/16/00
	11	6,472,258 B1	10/29/02	Adkisson et al.	438	192	11/13/00
	12	6,365,465 B1	04/02/02	Chan et al.	438	283	03/19/99
	13	6,064,589	05/16/00	Walker	365	149	05/05/98
	14	5,773,331	06/30/98	Solomon et al.	438	164	12/17/96
	15	5,677,550	10/14/97	Lee	257	69	04/15/93
	16	5,436,506	07/25/95	Kim et al.	257	347	10/12/93

EXAMINER | DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	17	5,349,228	09/20/94	Neudeck et al.	257	365	12/07/93
	18	5,273,921	12/28/93	Neudeck et al.	437	41	12/27/91
	19	3,755,012	08/28/73	George et al.	148	175	03/19/71

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICA-TION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	20							
	21							
	22							
	23							
	24							
	25							
	26							
	27							

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication , etc.)

	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
	29	Wann et al., "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.
	30	Yang et al., "Back-Gated CMOS on SOIAS for Dynamic Threshold Voltage Control," IEEE Transactions on Electron Devices, Vol. 44, No. 5, May 1997, pgs. 822-831.
	31	Assaderaghi et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pgs. 414-422.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

	32	Assaderaghi et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation," IEEE Electron Device Letters, Vol. 15, No. 12, December 1994, pgs. 510-512.
	33	Assaderaghi et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA, pgs. 33.1.1-33.1.4.
	34	Hsu et al., "Low-Frequency Noise Properties of Dynamic-Threshold (DT) MOSFET's," IEEE Electron Device Letters, Vol. 20, No. 10, October 1999, pgs. 532-534.
	35	Wong, H.-S. Philip, "Field Effect Transistors – From Silicon MOSFETS to Carbon Nanotube FETs," Proc. 23rd International Conference on Microelectronics (Miel 2002), Vol. 1, NIS, Yugoslavia, 12-15 May, 2002, pgs. 103-107.
	36	Brown et al., "Intrinsic Fluctuations in Sub 10-nm Double-Gate MOSFETs Introduced by Discreteness of Charge and Matter," IEEE Transactions on Nanotechnology, Vol. 1, No. 4, December 2002, pgs. 195-200.
	37	Denton et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate," IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511.
	38	Doris et al., "Extreme Scaling with Ultra-Thin Si Channel MOSFETs," IBM Semiconductor Research and Development Center (SRDC), Microelectronics Division, Hopewell Junction, NY 12533, pgs. 10.6.1-10.6.4.
	39	Choi et al., "Nanoscale Ultrathin Body PMOSFETs With Raised Selective Germanium Source/Drain," IEEE Electron Device Letters, Vol. 22, No. 9, September 2001, pgs. 447-448.
	40	Uchida et al., "Experimental Evidences of Quantum-Mechanical Effects on Low-field Mobility, Gate-channel Capacitance, and Threshold Voltage of Ultrathin Body SOI MOSFETs," Advanced LSI Technology Laboratory, Toshiba Corp., 8 Shinsugita-cho, Isogo-ku Yokohama 235-8522, Japan, pgs. 29.4.1-29.4.4.
	41	Ren et al., "An Experimental Study on Transport Issues and Electrostatics of Ultrathin Body SOI pMOSFETs," IEEE Electron Device Letters, Vol. 23, No. 10, October 2002, pgs. 609-611.
	42	Colinge et al., "Silicon-On-Insulator 'Gate-All-Around Device'," IMEC, Kapeldreef 75, 3030 Leuven, Belgium, pgs. 25.4.1-25.4.4.
	43	Hergenrother et al., "50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO_2 and $A1_2O_3$ Gate Dielectrics," Agere Systems, Murray Hill, NJ 07974, USA, pgs. 3.1.1-3.1.4.
	44	Hokazono et al., "14 nm Gate Length CMOSFETs Utilizing Low Thermal Budget Process with Poly-SiGe and Ni Salicide," SoC Research & Development Center, Process & Manufacturing Engineering Center, [2]System LSI Division, Toshiba Corporation Semiconductor Company, 8 Shinsugita-cho, Isogo-ku, Yokohama, Kanagawa 235-8522, Japan, pgs. 27.1.1-27.1.4.
	45	Schulz et al., "50-nm Vertical Sidewall Transistors With High Channel Doping Concentrations," Infineon Technologies AG, Corporate Research, D-81730 Munich, Germany, pgs. 3.5.1-3.5.4.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

	46	Fung et al., "Gate length scaling accelerated to 30nm regime using ultra-thin film PD-SOI Technology," IBM Microelectronics Semiconductor Research and Development Center (SRDC), pgs. 29.3.1-29.3.4.
	47	Narasimha et al., "High Performance Sub-40nm CMOS Devices on SOI for the 70nm Technology Node," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533, USA, pgs. 29.2.1-29.2.4.
	48	Hisamoto, Digh, "FD/DG-SOI MOSFET – a viable approach to overcoming the device scaling limit," Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185-8601, Japan, pgs. 19.3.1-19.3.4.
	49	Kedzierski et al., "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, 94720, USA, pgs. 3.4.1-3.4.4.
	50	Oh et al., "50 nm Vertical Replacement-Gate (VRG) pMOSFETs," Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974, USA, pgs. 3.6.1-3.6.4.
	51	Pidin et al., "A Notched Metal Gate MOSFET for sub-0.1 μm Operation," Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan, pgs. 29.1.1-29.1.4.
	52	Tavel et al., "High Performance 40nm nMOSFETs With HfO_2 Gate Dielectric and Polysilicon Damascene Gate," France Telecom R&D, B.P. 98, 38243 Meylan, France, pgs. 17.1.1-17.1.4.
	53	Krivokapic et al., "Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage," AMD, Technology Research Group, M/S 143, One AMD Place, Sunnyvale, CA 94088-3453, USA, pgs. 10.7.1-10.7.4.
	54	Monfray et al., "SON (Silicon-On-Nothing) P-MOSFETs with totally silicided ($CoSi_2$) Polysilicon on 5nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels," ST Microelectronics, 850, rue J.Monnet, 38921 Crolles, France, pgs. 10.5.1-10.5.4.
	55	Yang et al., "25 nm CMOS Omega FETs," Taiwan Semiconductor Manufacturing Company, No. 6, Li-Hsin Rd. 6, Science-Based Industrial Park, Hsin-Chu, Taiwan, ROC, pgs. 10.3.1-10.3.4.
	56	Wong et al., "Design and Performance Considerations for Sub-0.1 μm Double-Gate SOI MOSFET's," I.B.M. Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 30.6.1-30.6.4.
	57	Wong et al., "Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation," IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 15.2.1-15.2.4.
	58	Guarini et al., "Triple-Self-Aligned, Planar Double-Gate MOSFETs: Devices and Circuits," IBM T.J. Watson Research Center, Yorktown Heights, New York 10598, U.S.A., pgs. 19.2.1-19.2.4.
	59	Solomon et al., "Two Gates Are Better Than One," IEEE Circuits & Devices Magazine, January 2003, pgs. 48-63.
	60	Cheng et al., "The Impact of High-κ Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 7, July 1999, pgs. 1537-1544.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

	61	Oh et al., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs," IEEE Electron Device Letters, Vol. 21, No. 9, September 2000, pgs. 445-447.
	62	Ieong et al., "High Performance Double-Gate Device Technology Challenges and Opportunities," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY, USA, pgs. 492-495.
	63	Chang et al., "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 31.2.1-31.2.4.
	64	Wong et al., "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," IBM T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 16.6.1-16.6.4.
	65	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) with Low Threshold Voltage, High Drive Current, and Uniform Electrical Characteristics," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.2.1-29.2.4.
	66	Samavedam et al., "Dual-Metal Gate CMOS with HfO_2 Gate Dielectric," Motorola Digital DNA™ Laboratories, 3501 Ed Bluestein Blvd., MD:K10, (*AMD), Austin, TX 78721, USA, pgs. 17.2.1-17.2.4.
	67	Fossum et al., "Speed Superiority of Scaled Double-Gate CMOS," IEEE Transactions on Electron Devices, Vol. 49, No. 5, May 2002, pgs. 808, 809, 811.
	68	Lee et al., "Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy," Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, USA, pgs. 3.5.1-3.5.4.
	69	Polishchuk et al., "Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion," IEEE Electron Device Letters, Vol. 22, No. 9, September 2001, pgs. 444-446.
	70	Yeo et al., "Dual-Metal Gate CMOS Technology with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electron Device Letters, Vol. 22, No. 5, May 2001, pgs. 227-229.
	71	Wakabayashi et al., "A Dual-Metal Gate CMOS Technology Using Nitrogen-Concentration-Controlled TiNx Film," IEEE Transactions on Electron Devices, Vol. 48, No. 10, October 2001, pgs. 2363-2369.
	72	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) Technology for Very Low Voltage Operation of Under 0.7 V," IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 422-428.
	73	Matsuo et al., "High Performance Damascene Gate CMOSFETs with Recessed Channel Formed by Plasma Oxidation and Etching Method (RC-POEM)," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 17.5.1-17.5.4.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

	74	Ducroquet et al., "Full CMP Integration of CVD TiN Damascene Sub-0.1-μm Metal Gate Devices For ULSI Applications," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1816-1821.
	75	Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pgs. 25-27.
	76	Lindert et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, pgs. 487-489.
	77	Choi et al., "A Spacer Patterning Technology for Nanoscale CMOS," IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 436-441.
	78	Li et al., "Damascene W/TiN Gate MOSFETs With Improved Performance for 0.1-μm Regime," IEEE Transactions on Electron Devices, Vol. 49, No. 11, November 2002, pgs. 1891-1896.
	79	Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pgs. 880-886.
	80	Pei et al., "FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling," IEEE Transactions on Electron Devices, Vol. 49, No. 8, August 2002, pgs. 1411-1419.
	81	Hisamoto et al., "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pgs. 2320-2325.
	82	Chang et al., "FinFET Scaling to 10nm Gate Length," Strategic Technology, Advanced Micro Devices, Inc., Sunnyvale, CA 94088, USA, pgs. 10.2.1-10.2.4
	83	Choi et al., "FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 10.4.1-10.4.4.
	84	Lindert et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, pgs. 487-489.
	85	Huang et al., "Sub 50-nm FinFET: PMOS," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720, USA, pgs. 3.4.1-3.4.4.
	86	Choi et al., "Sub-20nm CMOS FinFET Technologies," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 19.1.1-19.1.4.
	87	Kedzierski et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," IBM Semiconductor Research and Development Center (SRDC), Research Division, T J Watson Research Center, Yorktown Heights, NY 10598, pgs. 10.1.1-10.1.4.
	88	Lin et al., "High-Performance P-Channel Schottky-Barrier SOI FinFET Featuring Self-Aligned PtSi Source/Drain and Electrical Junctions," IEEE Electron Device Letters, Vol. 24, No. 2, February 2003, pgs. 102-104.
	89	Lee et al., "Hydrogen Annealing Effect on DC and Low-Frequency Noise Characteristics in CMOS FinFETs," IEEE Electron Device Letters, Vol. 24, No. 3, March 2003, pgs. 186-188.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/3 US	APPLICATION NO. 10/719,119
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**		FILING DATE- November 21, 2003	

	90	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1μm Regime," Microelectronics Engineering Laboratory, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.3.1-29.3.4.
	91	Yagishita et al., "Improvement of Threshold Voltage Deviation in Damascene Metal Gate Transistors," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1604-1611.
	92	Yahishita et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 μm Regime," IEEE Transactions on Electron Devices, Vol. 47, No. 5, May 2000, pgs. 1028-1034.
	93	Kimura et al., "Short-Channel-Effect-Suppressed Sub-0.1-μm Grooved-Gate MOSFET's with W Gate," IEEE Transactions on Electron Devices, Vol. 42, No. 1, January 1995, pgs. 94-100.
	94	Tanaka et al., "Simulation of Sub-0.1-μm MOSFET's with Completely Suppressed Short-Channel Effect," IEEE Electron Device Letters, Vol. 14, No. 8, August 1993, pgs. 396-399.
	95	Tanaka et al., "A Sub-0.1-μm Grooved Gate MOSFET with High Immunity to Short-Channel Effects," Central Research Laboratory, Hitachi, Ltd., 1-280 Higashi-koigakubo, Kokubunji, Tokyo 185, Japan, pgs. 21.1.1-21.1.4.
	96	Sunouchi et al., "Double LDD Concave (DLC) Structure for Sub-Half Micron MOSFET," ULSI Research Center, Toshiba Corporation, 1, Komukai, Saiwai-ku, Kawasaki 210, Japan, pgs. 226-228.
	97	Hackler, Sr., Douglas R., "TMOS: A Novel Design for MOSFET Technology," A Thesis Presented in Partial Fulfillment of the Requirements for the Degree of Master of Science with a Major in Electrical Engineering in the College of Graduate Studies, University of Idaho, October 1999, 126 pgs.
	98	
	99	
	100	
	101	
	102	
	103	
	104	
	105	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.